	/	OIPE							
•	\bot	MAR 0 1 2004				· · · · · · · · · · · · · · · · · · ·			 -
FORM PTO-1 (REV. 7-80)	ORM PTO-1449 REV. 7-80) PAGENIA PATENT AND TRADEMARK OFFICE ATTY. DOCKET NO. 51764/2 APPLICATION NO 10/615,004					ION NO.			
	THE TAX OF THE PROPERTY OF THE								
									
Title: INFINITE IMPULSE RESPONSE MULTIPLIERLESS DIGITAL FILTER ARCHITECTURE				FILING DATE- July 8, 2003					
U.S. PATENT D	OCU	MENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME		CLASS	SUBCLASS	FILING IF APPR	DATE OPRIATE
EXAMINER	EXAMINER DATE CONSIDERED								
EXAMINER: In conformance and	nitial if	reference considered, onsidered. Include cop	whether or not cit	ation is in conformation wit h next communication to ap	h MPI plican	P609. Dra t.	w line throug	h citation i	f not in
FOREIGN PAT				·					
		DOCUMENT PUBLICA- COUNTRY / PATENT OFFICE		ICE	E CLASS	SUBCLASS		TRANSLATION	
		NUMBER	TION DATE	COUNTRY / PATENT OFFI		CLASS	- SODEDING	YES	NO
									0
OTHER DOCU	MENT	'S (Including Author, Titl	e. Date. Relevant Pa	nges, Place of Publication, etc.))		···		
AD	1	Yu et al., "New Nat	ural Selection Pr	ocess and Chromosome Er		g for the D	esign of Mul	tiplierless	Lattice
1	2	QMF Using Genetic Algorithm," 2001 IEEE, pgs. 1273-1276. Sriranganathan et al., "Design of 2-D Multiplierless FIR Filters Using Genetic Algorithms," Genetic Algorithms in Engineering Systems: Innovations and Applications 12-14 September 1995, Conference Publication No. 414, © IEE, 1995, pgs. 282-286.							
	3	Bhattacharya et al., "Multiplierless Implementation of Recursive Digital Filters Using a Class of Low Sensitivity Structures," International Symposium on Signal Processing and its Applications (ISSPA), Kuala Lumpur, Malaysia, 13-16 August, 2001, Organized by the Dept. of Microelectronics and Computer Engineering, UTM,							
	4	Malaysia and Signal Processing Research Centre, QUT, Australia, 2001 IEEE, pgs. 611-614. Lee et al., "GA-based design of multiplierless 2-D state-space digital filters with low roundoff noise," IEE Proc							
	5	Circuits Devices Syst., Vol. 145, No. 2, April 1998, pgs. 118-124. Lee et al., "GA-Based Design of Multiplierless 2-D Digital Filters with Very Low Roundoff Noise," Proceedings of IEEE Asia Pacific Conference on Circuits and Systems '96, November 18-21, 1996, Seoul, Korea, 1996 IEEE, pgs. 223-226.							
	6	Bhattacharya et al., "Multiplierless Implementation of Bandpass and Bandstop IIR Digital Filters," Institute of Signal Processing, Tampere University of Technology, P. O. Box 553, Tampere, FIN 33101, Finland, 2002 IEEE, pgs. III-3184-III-3187.							
	7	Bhattacharya et al., "Multiplierless Implementation of Recursive Digital Filters Based on Coefficient Translation Methods in Low Sensitivity Structures," Tampere International Center for Signal Processing, Tampere University of Technology, P. O. Box 553, Tampere, FIN 33101, Finland, 2001 IEEE, pgs. II-697-II-700.							
EXAMINER		MA =			,		CONSIDER		

EXAMINER: Initial if reference considered, whether or not citation is in conformation with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Sheet 2 of 3						
FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 51764/2	APPLICATION NO. 10/615,004			
INFORMATION DISCLOSU	FORMATION DISCLOSURE CITATION		APPLICANT - Tamal Bose et al.			
	SE RESPONSE MULTIPLIERLESS ARCHITECTURE	FILING DATE- July 8, 2003	·			

AD	8	Cemes et al., "Genetic approach to design of multiplierless FIR filters," ELECTRONICS LETTERS, 25th November 1993, Vol. 29, No. 24, pgs. 2090-2091.		
	9	Mao et al., "Design and Multiplierless Implementation of Two-Channel Biorthogonal IIR Filter Banks with Low System Delay," Dept. of Electrical and Computer Engineering, University of Victoria, Victoria, B.C., Canada V8W 3P6, Dept. of Electrical and Electronic Engineering, University of Hong Kong, Pokfulam Road, Hong Kong, 2001 IEEE, pgs. II-465-II-468.		
;	10	Hounsell et al., "Evolutionary Design and Adaptation of Digital Filters Within an Embedded Fault Tolerant Hardware Platform," Department of Electronics and Electrical Engineering, The University of Edinburgh, King's Buildings, Mayfield Rd, Edinburgh EH9 3JL, 2001 IEEE, pgs. 127-135.		
	11	Oh et al., "Design of Discrete Coefficient FIR and IIR Digital Filters with Prefilter-Equalizer Structure Using Linear Programming," IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing, Vol. 47, No. 6, June 2000, pgs. 562-565.		
	12	Wiatr et al., "Implementation of real time image convolutions in FPGA structures," pgs. 1-10.		
	13	Wiatr et al., "Constant Coefficient Multiplication in FPGA Structures," AGH Technical University, Institute of Electronics, Mickiewicza 30, 30-059 Kraków, Poland, pgs. 1-8.		
	14	Venkatachalam et al., "Adaptive Linear Prediction with Power-of-Two Coefficients," Electrical & Computer Engineering, Utah State University, Logan, UT 84322-4120, Electrical & Computer Engineering, University of Colorado, Boulder, CO 80309-0425, 2001 IEEE, pgs. 533-537.		
	15	Thamvichai et al., "Design of 2-D Multiplierless Filters Using the Genetic Algorithm," Electrical & Computer Engineering, University of Colorado, Boulder, CO 80309, Electrical & Computer Engineering, Utah State University, Logan, UT 84322-4120, 2001 IEEE, pgs. 588-591.		
	16	Jamro et al., "FPGA Implementation of Addition as a Part of the Convolution," AGH Technical University, Institute of Electronics, Mickiewicza 30, 30-059 Kraków, Poland, pgs. 1-9.		
	17	Jamro et al., "Convolution Operation Implemented in FPGA Structures for Real-Time Image Processing," AGH Technical University, Institute of Electronics, pgs. 1-6.		
.1	18	Ghanekar et al., "Implementation of Recursive Filters Using Highly Quantized Periodically Time-Varying Coefficients," Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, MA 01003, 1991 IEEE, pgs. 1625-1628.		
	19	Hartnett et al., "IIR Filters with Reduced Multipliers Using Cyclotomic Polynomial Numerators," U. S. Coast Guard Academy, New London, CT 06320, University of Rhode Island, Kingston, RI 02881, 1992 IEEE, pgs. IV-321-324.		
	20	Milić et al., "Design of Multiplierless Elliptic IIR Filters," Mihajlo Pupin Institute, Volgina 15, 11000 Belgrade, Yugoslavia, IRITEL Institute, Batajnicki put 23, 11080 Belgrade, Yugoslavia, 1997 IEEE, pg. 2201-2204.		
\mathfrak{D}	21	Lian, "FPGA Implementation of High Speed Multiplierless Frequency Response Masking FIR Filters," Electrical Engineering Department, National University of Singapore, 10 Kent Ridge Crescent, Singapore 119260, 2000 IEEE, pgs. 317-325.		
EXAMINER	•	DATE CONSIDERED		

EXAMINER: Initial if reference considered, whether or not citation is in conformation with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Sheet 3 of 3		•			
FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 51764/2	APPLICATION NO. 10/615,004		
INFORMATION DISCLOSURE CITATION		APPLICANT - Tamal Bose et al.			
Title: INFINITE IMPULSE RESPONSE MULTIPLIERLESS DIGITAL FILTER ARCHITECTURE		FILING DATE- July 8, 2003			

AD	22	Lutovac et al., "Approximate Linear Phase Multiplierless IIR Halfband Filter," IEEE Transactions on Signal Processing Letters, Vol. 7, No. 3, March 2000, pgs. 52-53.
1	23	Chan et al., "Multiplierless Perfect Reconstruction Modulated Filter Banks with Sum-of-Powers-of-Two Coefficients," IEEE Signal Processing Letters, Vol. 8, No. 6, June 2001, pgs. 163-166.
	24	Milić et al., "Design of Multiplierless Elliptic IIR Filters with a Small Quantization Error," IEEE Transactions on Signal Processing, Vol. 47, No. 2, February 1999, pg. 469-479.
AD	25	Thamvichai et al., "Design of 2-D Multiplierless IIR Filters Using the Genetic Algorithm," IEEE Transactions on Circuits and Systems—I: Fundamental Theory and Applications, Vol. 49, No. 6, June 2002, pgs. 878-882.
,	26	
· · · · · · · · · · · · · · · · · · ·	27	·
	28	
······································	29	
	30	
	31	
	32	·
	33	
<u>-</u>	34	
·· · · · · · · · · · · · · · · · · · ·	35	
•	36	
	37	
	38	
	39	
	40	
	41	
	42	
	43	
FYAMINER		DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformation with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.